REMARKS/ARGUMENTS

Applicants received the Office Action dated October 2, 2003, in which the Examiner: (1) objected to the Abstract; (2) objected to the drawings; (3) objected to claim 9; (4) rejected claims 1-3, 7-11, and 15-20 as obvious over Mallick (U.S. Pat. No. 5,752,014) in view of "Intel IA-64 Architecture Software Developer's Manual Volume 1: IA-64 Application Architecture (referred to as "Intel Volume 1"); and (5) rejected claims 4-6, 12-14 and 21-22 as obvious over Mallick in view of Intel Volume 1 and "Intel Itanium Architecture Software Developer's Manual Volume 3: Instruction Set Reference (referred to as "Intel Volume 3"). In this Response, Applicants cancel claims 2-3, 10-11, 14, and 19-20 and amend claims 1, 4-5, 7-9, 12-13, 15-16, 18, and 21-22. Based on the amendments and arguments contained herein, Applicants submit that all pending claims are allowable and respectfully requests a Notice of Allowance.

I. The Objection to the Abstract

Applicants amend the Abstract to address the Examiner's concern with reference to the phrase "problems noted above" as well as to ensure the Abstract comports with the scope of the disclosed and claimed subject matter.

II. The Drawing Objection

The Examiner noted that the specification refers to reference numeral "16" with regard to the L1 cache, but the drawings identify the L1 cache as "116." Applicants hereby address the Examiner's concern by amending the specification to refer to reference numeral 116.

III. Objection of Claim 9

The Examiner noted that claim 9 omitted the word "queue." This word has been added to the claim.

IV. The Art Rejections

Applicants amend claim 1 to specify, among other features, that "static branch prediction instructions comprise a plurality of groups of static branch prediction bits, each group being configurable to provide prediction information for a separate conditional branch instruction." The Examiner correctly concedes that Mallick does not teach separate static branch prediction instructions. Further,

Intel Volume 1 does not teach a branch prediction instruction that comprises a group of prediction bits in which each group is configurable to provide prediction information for a separate branch instruction. At most, Intel Volume 1 discloses a branch prediction instruction that provides prediction information for only one branch conditional instruction. Intel Volume 3 discloses a branch prediction instruction that includes an operand that "specifies the address of **the** branch instruction to which this prediction information applies." Intel Volume 3, page 3:28 (emphasis added). In referring to "the" branch instruction, the Intel Volume 3 document does not teach or suggest that each branch prediction instruction can provide prediction information regarding more than one branch instruction. At least for this reason, claim 1 is patentable.

All claims that depend on or from claim 1 are patentable at least for the same reason as claim 1. Applicants amend claim 4 to depend from claim 1 and to specify that each group of branch prediction bits comprises a pair of bits. Applicants amend claim 5 to depend from claim 1. Further, claims 1, 4, 5, 7 and 8, as well as claims 12, 13, 15, 16, 21 and 22 have been amended to use the verb "comprise" instead of "include" to ensure the claims are afforded their full breadth.

Claim 9, as amended, refers to a static branch prediction instruction that provides "separate static branch prediction information about a plurality of conditional branch instructions." As explained above, none of the art of record teaches or suggests this feature. For at least this reason, claim 9 and all claims that depend on or from claim 9 are allowable.

Claim 12 has been amended to correct an antecedent basis issue regarding the "static branch prediction bits" and also to specify that the branch prediction information for each conditional branch instruction comprises a pair of bits. The dependency link of claim 13 has been changed to claim 9. Claim 15 has been amended to clean up some language.

Applicants amend independent method claim 18 to specify "including a static branch predictor software instruction in a program, said branch prediction software instruction including branch prediction information configurable to pertain

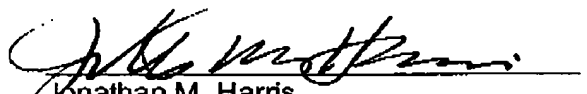
to a plurality of conditional branch instructions in the program." As explained above, none of the art of record teaches or suggests this feature. For at least this reason, claim 18 and all claims that depend on or from claim 18 are allowable.

References to labels "(a)" through "(d)" have been removed from claim 18 and dependent 19 so as not imply any particular order to the limitations in the claimed method. These amendments do not narrow the scope of the claims.

CONCLUSION

Applicants respectfully request that a timely Notice of Allowance be issued in this case. If any fees or time extensions are inadvertently omitted or if any fees have been overpaid, please appropriately charge or credit those fees to Hewlett-Packard Company Deposit Account Number 08-2025 and enter any time extension(s) necessary to prevent this case from being abandoned.

Respectfully submitted,



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ABSTRACT

A computer system comprises a processor that comprises a hardware branch predictor and software instructions executed by the processor. The software instructions comprise conditional branch instructions and separate static branch prediction instructions. The static branch prediction instructions comprise a plurality of groups of static branch prediction bits, each group being configurable to provide prediction information for a separate conditional branch instruction.